

WHAT IS CLAIMED IS:

1. An associative memory comprising:
 - a plurality of match lines, from a first match line to an n-th match line, where n is an integer greater than 1, wherein a plurality of associative memory cells being connected to each match line;
 - a first match line pre-charge circuit that pre-charges the first match line;
 - a first sense amplifier that detects a potential of the first match line;
- 10 an m-th match line pre-charge circuit that pre-charges an m-th match line, where m is a number of integers from 2 to n;
 - a control circuit for the m-th match line that operates the m-th match line pre-charge circuit, only when the potential of the (m-1)-th match line detected by the (m-1)-th sense amplifier is a potential when stored data in the associative memory cell connected to the (m-1)-th match line agrees with search data; and
 - 15 an m-th sense amplifier that detects a potential of the m-th match line.
- 20 2. The associative memory according to claim 1, further comprising an m-th search bus driving circuit that supplies search data to associative memory cells connected to the m-th match line, after the m-th match line has been pre-charged.
- 25 3. The associative memory according to claim 2, further

comprising:

an (m-1)-th search bus driving circuit that supplies search data to the associative memory cells connected to the (m-1)-th match line;

and

5 a delay circuit that supplies a search bus control signal for activating the (m-1)-th search bus driving circuit to the (m-1)-th search bus driving circuit, with predetermined timing delayed in order to activate the m-th search bus driving circuit.

10 4. The associative memory according to claim 1, further comprising:

 a first latch circuit that temporarily holds the potential of the (m-1)-th match line detected by the (m-1)-th sense amplifier, and supplies the potential to the m-th match line control circuit,

15 synchronously to the next clock pulse;

 an (m-1)-th search bus driving circuit that supplies search data to associative memory cells connected to the (m-1)-th match line;

 an m-th search bus driving circuit that supplies search data to associative memory cells connected to the m-th match line; and

20 a second latch circuit that temporarily holds a search bus control signal for activating the (m-1)-th search bus driving circuit, and supplies it to the m-th search bus driving circuit, synchronously to the next clock pulse, as a search bus control signal for activating the m-th search bus driving circuit,

25 wherein data search with respect to the associative memory

cells connected to the $(m-1)$ -th match line, and data search with respect to the associative memory cells connected to the m -th match line are carried out with a pipeline operation.

5 5. The associative memory according to claim 1, wherein both n and m are equal to 2.